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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Masashi NAKAMURA et al.
Serial No.	:	09/889,374
For	:	DIGITAL SIGNAL PROCESSING APPARATUS, SYSTEM THEREOF, AND EXTENSION FUNCTION PROVIDING METHOD
Filed	:	June 16, 2001
Examiner	:	Venkatanaray Perungavoor
Art Unit	:	2132

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APPELLANTS' BRIEF ON APPEAL

Mail Stop **APPEAL BRIEF-PATENTS**
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Sir:

This Brief of Applicants is submitted in triplicate in support of Applicants' appeal to the Board of Patent Appeals and Interferences from the Examiner's final rejection of all of the claims present in the above identified application. This Brief is timely filed following the filing of the Notice of Appeal and is accompanied by the requisite fee of $500.

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Real Party in Interest

Sony Corporation, a corporation of Japan, is the real party in interest by reason of the assignment from Applicants, recorded on July 16, 2001 at reel 012085, frame 0643.

Related Appeals and Interferences

As understood by Applicants' below-named attorney, there are no prior or pending appeals, interferences or judicial proceedings that may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of the Claims

This application was filed with claims 1-18. In the first Office Action mailed January 12, 2005, all claims were rejected as being anticipated by U.S. Patent 5,977,997 ("Vainsencher"). Applicants' amendment filed April 19, 2005 added to the independent claims the feature of enabling a block to be added to the bus or enabling a block connected to the bus to be changed, by way of the interface means.

The final rejection of May 27, 2005, from which this appeal is taken, once again rejected claims 1-18 for much the same reasons set out in the first Office Action of January 12, 2005. Applicants filed their amendment under 37 CFR 1.116 on August 3, 2005 to amend independent claims 1, 6, 10 and 15, thereby emphasizing that which should have been clear from the original claims, namely, that the "bus" to which all of the claimed "blocks" are coupled is a common bus.

The Advisory Action of August 18, 2005 noted that Applicants' amendment submitted under 37 CFR 1.116 had been entered but the Examiner nevertheless maintained his rejection. This appeal was filed on August 29, 2005.

Accordingly, the status of the claims is as follows:

Claims allowed: none

Claims canceled: none.

Claims rejected: claims 1-18.

Status of Amendments

The amendment filed August 3, 2005 under 37 CFR 1.116 was entered.

Summary of Claimed Subject Matter

Applicants' claimed invention is directed to a method and apparatus that enable functional blocks connected to a common bus in a signal processing system to be easily added or changed, while preventing information that may flow to a new block from being pirated. One environment for Applicants' invention is described as a digital television receiver that can be easily reconfigured to receive digital satellite broadcasts from communication satellites, from soon to be introduced "ground wave" (or terrestrial) broadcasts, or from a wide variety of television standards (e.g. MPEG, encryption, etc.). Heretofore, as shown in Fig. 1 of the present application, a bus 110 extended from a processor MPU 111 to a tuner 102, a demultiplexer 103, a video decoder 104, an audio decoder 105 and a graphics processor 106 (page 3, lines 15-22 of Applicants' specification). Of course, the MPU, provided central control over all of these blocks, but if the design of any block was to change, such as to accommodate a new transmission format or standard, the software written for the MPU would have to be rewritten (page 4, lines 8-27). If the blocks are connected to a standard bus, there is the probability that content information transferred over the bus could be easily pirated (page 5, lines 1-4). The present invention addresses and solves this problem faced by the prior art.

As summarized at page 7, lines 10-21,

> Elements necessary for a digital television receiver are structured as blocks and connected through a general purpose bus. Thus, by substituting only blocks, various types of digital television broadcasts that differ in carrier waves, modulating systems, and compressing systems can be handled. When an encryption encoder/decoder[r] circuit is disposed in an interface to which an extension plug-in card is attached, contents that are output from the interface can be protected.
>
> ***
>
> Thus, the developing efficiency of digital television receivers is improved. In addition, when a new service is started, by adding hardware, for the service, the device can easily handle the service. (page 9, lines 15-17).

Fig. 2 of the present application illustrates one embodiment of Applicants' claimed invention in the environment of a digital television receiver. Of course, the claimed invention has wider application than only digital television; and the claims are not limited solely to that environment. Several blocks 12-16 are connected to a bus 10, as is "host MPU block 11" (page 9, line 22 to page 10, line 4) (MPU means microprocessor unit – see page 3, line 18). Block 14 is an interface block "for connecting the receiver with an external device" and block 15 is a "plug-in interface block ... for connecting the receiver with hardware for an extension function" (page 10, lines 13-18). Advantageously, the MPU block sends to the other blocks high level commands that are general purpose commands that do not depend on hardware (page 13, lines 8-16) and these commands are interpreted and handled by the driver of each recipient block (page 13, lines 17-23).

Commands, streams and data are exchanged among the blocks through bus 10, such that the system formed of those blocks can be developed and designed for changing standards (page 14, line 20 to page 15, line 1). As an example, blocks that are used for satellite broadcasts can be changed to accommodate ground wave digital broadcasts when such ground wave digital broadcast systems are developed and eventually implemented; and additional blocks that may be

needed to receive and accommodate such ground wave digital broadcasts can be added to the basic system shown in Fig. 2 (Page 15, line 17 to page 16, line 18). New or changed blocks are incorporated into the system by way of plug-in interface block 15; and if the new or changed block needs a different driver, that driver may be stored in the memory of the block attached to the interface block (page 16, line 24 to page 17, line 5). As a result, the basic system readily improves its capability and can accommodate new or changed functionalities without significant redesign or serious hardware or software changes. And the use of high level commands makes it unnecessary to install new drivers in the MPU block (page 17, line 27 to page 18, line 2).

Fig. 7 illustrates another embodiment of the novel system, particularly adapted for use as a television receiver, with a common bus 30 to which several blocks, including a host MPU 21 is connected (the host is connected to the common bus through a bus controller 26). The blocks include an external interface block 33 and a plug-in interface block 35, the latter serving as in interface to connect an extension plug-in card 36 to the system (page 19, lines 20-22). The external interface block 33 "provides an interface with an external device" (page 21, lines 19-23) and the plug-in interface 35 "provides an extension function for receiving a new service" (page 22, lines 6-12). However, blocks 33 and 35 permit an external copying device to be easily connected to bus 30 and thus, without authorization, easily extract and copy information sent through the bus (page 25, lines 14-23). This pirating of information is prevented by the present invention by providing encryption encoders/decoders in the blocks connected to the bus 30 (page 25, line 24 to page 26, line 8). In particular, an encryption encoder/decoder 89 is disposed in the plug-in interface block 35 "so that data of contents that flow on the bus 30 is not leaked out from the plug-in interface 35" (page 26, lines 22-26). Consequently, when a new or changed block schematically illustrated as extension plug-in card 36 is connected to bus 30 through plug-in

interface 35, a new function can be accommodated with minimum risk of piracy (page 27, lines 8-17).

Grounds of Rejection to be Reviewed on Appeal

The Final Rejection here under appeal rejects claims 1-18, all the claims present in this application. This honorable Board is asked to review the rejection under 35 USC 102 of claims 1-18 as being anticipated by U.S. Patent 5,977,997 (Vainsencher).

Argument

The Disclosure of Vainsencher

Vainsencher is directed to "a highly integrated, single chip computer system having not only a central-processing unit (CPU) but also specialized coprocessors" (see title and col. 2, lines 9-12). The single chip 200 has an inter-processor bus coupled between the CPU and the coprocessors as well as a main CPU bus for coupling the CPU to the memory interface (col. 2, lines 37-43). Vainsencher's single integrated circuit chip is shown in Fig. 2 as including several busses that interconnect the various operating blocks, including coprocessor bus 210, I/O bus 212, main CPU bus 214, video bus 242 and graphics bus 244.

A primary memory interface 218, coupled to the video bus and to the graphics bus, couples the chip 200 to main memory 104 through a first memory bus 220; and an auxiliary memory interface 224 couples the chip to main memory 104 through a second memory bus 226 (col. 5, lines 14-22). Each of these memory interfaces includes an encrypter/decrypter to encrypt data sent to the main memory and to decrypt data received from the main memory. In addition, chip 200 includes a stream I/O interface 230 that is coupled by a separate stream bus 234 to I/O bus 212 and to main CPU bus 214 (col. 5, lines 31-34). Interface 230 has a decrypter 232 to

decrypt incoming data from a peripheral device "for use internal to the chip" (col. 5, lines 36-38).

A video encoder 240 receives video information from display controller 238 to drive an external display device 108 (col. 5, lines 52-64). While Vainsencher contends that the encryption and decryption apparatus provided in chip 200 is useful to enhance the security for the computer program or data that the chip utilizes or produces, it is noted that the point at which the video data (or content information) can be readily pirated, namely, the video data produced by video encoder 240, is not described as being encrypted: "encoder 240 generates synchronization information and produces digital video waveforms with PAL NTSC synchronization" (col. 5, lines 62-64). The flow diagrams shown in Figs. 3 and 4 make it clear that the software, or program, for chip 200 is encrypted, but there is no description of suggestion of encrypting the content information that is supplied to an external display device.

Vainsencher emphasizes the fact that his chip 200 is a single chip, highly integrated computer system. As such, Vainsencher does not contemplate the addition or change to any of the blocks illustrated in his Fig. 2. As a single, integrated chip, it would be highly unusual to change or add blocks because the chip would have to be completely reconstructed. Furthermore, Fig. 2 illustrates several busses to interconnect Vainsencher's several operating blocks within his chip. That is, there is no suggestion of a common bus to which all of his blocks are connected. Moreover, while Vainsencher shows a number of interfaces 218, 224 and 230, he clearly does not describe these interfaces as enabling blocks to be changed or added; nor does he guard against pirating content information that may be transferred through a common bus to a new block by encrypting such content information that would be transferred to that new block.

Notably, video encoder 240, which would supply content information to a display device external to chip 200, contains no encryption means.

The Final Rejection

Claims 1-4 and 10-13

Claims 1-4 and 10-13 are grouped together for the purpose of this appeal and stand or fall together.

Claim 1 is illustrative and recites, inter alia,

> "a common bus for connecting said host arithmetic operation processing block and said plurality of digital signal processing blocks;
>
> interface means coupled to said common bus to enable a block to be added to the common bus or to enable a block connected to the common bus to be changed; and
>
> means for encrypting data of a stream transferred through said common bus."

In attempting to demonstrate that Vainsencher anticipates claim 1, the Examiner, in his Final Rejection, refers to the paragraph bridging columns 2 and 3 of Vainsencher and the paragraph bridging columns 5 and 6 as disclosing Applicants' claimed "common bus." The former paragraph simply describes the blocks that make up the single chip computer system and that the computer software data is encrypted. The latter paragraph describes the several busses that are used to interconnect the various blocks in the single chip computer. There is no "common bus."

The Final Rejection relies on col. 5, lines 45-52 of Vainsencher as describing an "interface that is coupled to the bus and can enable blocks to be added and changed." However, as pointed out above in the description of Vainsencher, the very fact that Vainsencher describes a single chip computer system makes it clear that Vainsencher does not contemplate any addition or change to the blocks included in his system. To do so would require a complete

reconstruction of that chip. Furthermore, although Vainsencher shows interfaces 218, 224 and 230, these interfaces are connected to three separate busses 234, 212 and 214. These three separate busses cannot reasonably be construed as a "common bus." Thus, Vainsencher fails to disclose "a common bus" and he is incapable of adding a block to his non-existent common bus or changing a block.

Vainsencher describes encrypting program data, or software, used to control his CPU. But he fails to suggest encrypting "data of a stream transferred through said common bus." The only stream data found in Vainsencher is the video output supplied by video encoder 240; but this stream data is not encrypted. And video encoder 240 is not connected to a common bus so that there is no encryption of stream data "transferred through said common bus" as called for by Applicants' claim 1.

It is axiomatic, to anticipate a claimed invention under 35 USC 102, the reference relied upon for anticipation must describe each and every element recited by the claim. *Verdegaal Bros. v. Union Oil Co. of California,* 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); *In re Kalm*, 154 USPQ 10 (CCPA 1867); *In re Royka and Martin*, 180 USPQ 580 (CCPA 1974); *In re Lange*, 209 USPQ 288-293 (CCPA 1981); *Connell* v. *Sears Roebuck & Co.*, 220 USPQ 193-198 (Fed Cir. 1983); *Leinoff* v. *Lewis Milona & Sons*, 220 USPQ 845 (Fed. Cir. 1984); *Jamesbury Corp.* v. *Litton Industrial Products, Inc.*, 225 USPQ 253, 256 (Fed. Cir. 1985); *Ex parte DesGranges*, 162 USPQ 379, 382 (Bd of Pat. App. and Int. 1968). Note, particularly, section 2131 of the MPEP. Here, important limitations of claim 1 are not found in Vainsencher. Such limitations cannot be ignored. Consequently, Vainsencher cannot anticipate claim 1; and the rejection of claim 1 (and the rejections of claims 2-4 and 10-13) as set out in the Final Rejection here under appeal must be reversed.

Claims 5 and 14

For the purpose of this appeal, claims 5 and 14 constitute another group and stand or fall together. These claims depend from claims 1 and 10, respectively, and are patentably distinct from Vainsencher for the reasons discussed above. In addition, each of these claims recites,

> "said common bus is a general-purpose bus, and
>
> wherein each block connected to said common bus can be added or substituted."

Vainsencher describes several individual busses to interconnect the blocks in his single chip computer system. There is no common, general-purpose bus. Also, since Vainsencher discloses a single chip computer, it is clear he does not contemplate or expect to substitute or add to the blocks shown in his Fig. 2. The aforequoted elements recited in claims 5 and 14 thus find no correspondence in Vainsencher and, as a result, cannot be said to be anticipated by this reference. The Final Rejection of claims 5 and 14 should be reversed.

Claims 6-9 and 15-18

For the purpose of this appeal, claims 6-9 and 15-18 are grouped together and stand or fall together.

Claim 6 is illustrative and in addition to the elements found in claim 1, also recites,

> "means for encrypting the data of the stream that is output through said interface of the extension function providing medium when the data of the stream is transferred to the extension providing medium through said common bus."

This "means" is readable on plug-in interface 35 and encryption encoder/decoder 89 included therein, as shown in Fig. 9. It is this interface that outputs the encrypted data stream to what is described in Applicants' specification as an extension plug-in card that has an extension function, namely, the function of communicating stream data to the outside. Arguably, Vainsencher's video encoder 240 (Fig. 2) has an extension function because this is the only

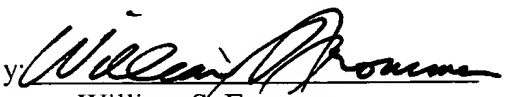
block that sends a data stream to the outside, i.e. to the display. But, there is no means in Vainsencher's video encoder that encrypts the content information supplied thereto.

Consequently, Vainsencher cannot anticipate claim 6 for the additional reason that the aforequoted element recited in this claim finds no correspondence in the disclosure of Vainsencher. Therefore, the Final Rejection of claim 6, as well as the Final Rejection of claims 7-9 and 15-18 should be reversed.

Conclusion

The subject matter defined by claims 1-18 includes elements that are neither described nor suggested by the Vainsencher patent relied upon by the Examiner to anticipate these claims. The Final Rejection fails to explain how Vainsencher, which clearly fails to describe important claim recitations, nevertheless anticipates Applicants' claims. The statute, controlling case law and the practice of the Office establish that the Examiner's rejection is in error. Accordingly, this Honorable Board should reverse the Examiner's Final Rejection and mandate the allowance of Applicants' claims.

Respectfully submitted,
FROMMER LAWRENCE & HAUG LLP

By 
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Appendix

Claims on Appeal

1. A digital signal processing apparatus, comprising:

a plurality of digital signal processing blocks and a host arithmetic operation processing block as functions necessary for processing a digital signal;

a common bus for connecting said host arithmetic operation processing block and said plurality of digital signal processing blocks;

interface means coupled to said common bus to enable a block to be added to the common bus or to enable a block connected to the common bus to be changed; and

means for encrypting data of a stream transferred through said common bus.

2. The digital signal processing apparatus as set forth in claim 1, wherein said plurality of digital signal processing blocks include encrypting/decrypting means for encrypting/decrypting the data of the stream transferred through said common bus.

3. The digital signal processing apparatus as set forth in claim 1, wherein the data of the stream contains video data and/or audio data.

4. The digital signal processing apparatus as set forth in claim 3, wherein the video data and/or the audio data has been compressed.

5. The digital signal processing apparatus as set forth in claim 1,

wherein said common bus is a general-purpose bus, and

wherein each block connected to said common bus can be added or substituted.

6. A digital signal processing apparatus, comprising:

a plurality of digital signal processing blocks and a host arithmetic operation processing block as functions necessary for processing a digital signal;

a common bus for connecting said host arithmetic operation processing block and said plurality of digital signal processing blocks;

interface means coupled to said common bus to enable a block to be added to said common bus or to enable a block connected to said common bus to be changed; and

means for encrypting the data of the stream that is output through said interface of the extension function providing medium when the data of the stream is transferred to the extension providing medium through said common bus.

7. The digital signal processing apparatus as set forth in claim 6, wherein said interface of the extension function providing medium includes encrypting/decrypting means for encrypting/decrypting data of a stream that is output through said interface of the extension function providing medium.

8. The digital signal processing apparatus as set forth in claim 6, wherein the data of the stream contains video data and/or audio data.

9. The digital signal processing apparatus as set forth in claim 8, wherein the video and/or audio data has been compressed.

10. A digital signal processing method, comprising the steps of:

structuring functions necessary for processing a digital signal as a plurality of digital signal processing blocks and a host arithmetic operation processing block;

connecting the host arithmetic operation processing block and the plurality of digital signal processing blocks through a common bus;

providing a means coupled to said common bus to enable a block to be added to said common bus or to enable a block connected to said common bus to be changed; and

encrypting data of a stream transferred through the common bus.

11. The digital signal processing method as set forth in claim 10, wherein the plurality of digital signal processing blocks include a step for encrypting/decrypting the data of the stream transferred through the common bus.

12. The digital signal processing method as set forth in claim 10, wherein the data of the stream contains video data and/or audio data.

13. The digital signal processing method as set forth in claim 12, wherein the video data and/or the audio data has been compressed.

14. The digital signal processing method as set forth in claim 10,

wherein the common bus is a general-purpose bus, and

wherein each block connected to the common bus can be added or substituted.

15. A digital signal processing method, comprising the steps of:

structuring functions necessary for processing a digital signal as a plurality of digital signal processing blocks and a host arithmetic operation processing block;

connecting the host arithmetic operation processing block and the plurality of digital signal processing blocks through a common bus;

providing a means coupled to said common bus to enable a block to be added to said common bus or to enable a block connected to said common bus to be changed; and

encrypting the data of the stream that is output through the interface of the extension function providing medium when the data of the stream is transferred to the extension function providing medium through the common bus.

16. The digital signal processing method as set forth in claim 15, wherein the interface of the extension function providing medium includes a step for encrypting/decrypting data of a stream that is output through the interface of the extension function providing medium.

17. The digital signal processing method as set forth in claim 15, wherein the data of the stream contains video data and/or audio data.

18. The digital signal processing method as set forth in claim 17, wherein the video data and/or the audio data has been compressed.